This listing of claims will replace all prior versions, and listings, of claims to the application:

1. (Previously Presented): An analog-to-digital converter with reduced parasitic capacitance on the input during a sampling operation, comprising:

a charge-redistribution, binary-weighted switched-capacitor array having a plurality of array capacitors that each have a commonly connected plate interfaced to a first common node and a switched plate, said switched plate operable to be switched between first and second reference voltages during a redistribution phase and selected ones of said capacitors additionally operable to be switched to the input during a sampling phase;

each of said array capacitors having a parasitic capacitance associated therewith;

a compensation capacitor having a common plate connected to said first common node and a switched plate operable to be switched to the input during the sampling phase and to said first reference voltage during the redistribution phase, the parasitic capacitance thereof less than the parasitic capacitance of the combination of all of said non-selected ones of said array capacitors;

a comparator for comparing the voltage on said first common node to a compare reference voltage during the redistribution phase; and

a successive approximation controller for switching the switched plate of said array capacitors between said first and second reference voltages in accordance with a successive approximation algorithm during the redistribution phase.

2. (Previously Presented): The analog-to-digital converter of Claim 1, wherein said compensation capacitor has a value that is substantially equal to the value of the equivalent capacitance of all of said non-selected array capacitors connected to said first common node.

3. (Previously Presented): The analog-to-digital converter of Claim 2, wherein said switched-capacitor array comprises a bridge capacitor array, including:

at least first and second array sections;

said first array section associated with said first common node and said second array section associated with a second common node;

said second common node separated from said first common node by a series capacitor;

said non-selected array capacitors inclusive of said array capacitors in said second section; and

wherein said compensation capacitor has a value equal to the equivalent capacitance loaded on said first common node from said non-selected array capacitors in said second section.

4. (Original): The analog-to-digital converter of Claim 3, wherein said compensation capacitor has a parasitic capacitance proportionally equal to the parasitic capacitance of each of said array capacitors based on the relative values thereof.

5.(Previously Presented): The analog-to-digital converter of Claim 3, wherein at least one of said array capacitors in said first section comprises one of said non-selected array capacitors.

6. (Previously Presented): The analog-to-digital converter of Claim 5, wherein the at least one of said array capacitors in said first section that comprises one of said non-selected array capacitors comprises the smallest capacitance value in said first section.

7. (Original): The analog-to-digital converter of Claim 1, wherein said first reference voltage comprises system ground.

8. (Original): The analog-to-digital converter of Claim 1, wherein said compare reference voltage comprises a common mode reference voltage.

9. (Currently Amended): The analog-to-digital converter of Claim 8, wherein said common mode <u>reference</u> voltage is generated by a low impedance common mode driver.

10. (Previously Presented): The analog-to-digital converter of Claim 9, wherein said low impedance common mode driver is operable to drive said first common node during the sampling phase.

11. (Original): The analog-to-digital converter of Claim 1, wherein said successive approximation controller is operable to switch all of the switched plates of said array capacitors and the switched plate of said compensation capacitor to said first reference voltage substantially immediately after the sampling phase during a hold phase, and then selectively switching the switched plates of said array capacitors to said second reference voltage in accordance with the successive approximation algorithm and then testing the output of said comparator.

12. (Original): The analog-to-digital converter of Claim 11, wherein said first reference voltage comprises system ground.

14. (Currently Amended): A method for converting data with an analog-to-digital converter with reduced parasitic capacitance on the input during a sampling operation, comprising the steps of:

forming a charge-redistribution, binary-weighted switched-capacitor array having a plurality of array capacitors that each have a commonly connected plate interfaced to a first common node and a switched plate, the switched plate operable to be switched between first and second reference voltages during a redistribution phase and selected ones of the capacitors additionally operable to be switched to the input during a sampling phase;

each of the array capacitors having a parasitic capacitance associated therewith;

connecting a common plate of a compensation capacitor to the first common node and switching a switched plate of the compensation capacitor to the input during the sampling phase and to the first reference voltage during the redistribution phase, the parasitic capacitance thereof less than the parasitic capacitance of the combination of all of the non-selected ones of the array capacitors;

comparing with a comparator the voltage on the first common node to a compare reference voltage during the redistribution phase; and

switching with a successive approximation controller the switched plate of the array capacitors between the first and second reference voltages in accordance with a successive approximation algorithm during the redistribution phase.

15. (Previously Presented): The method of Claim 14, wherein the compensation capacitor has a value that is substantially equal to the value of the equivalent capacitance of all of the non-selected array capacitors connected to the first common node.

16. (Currently Amended): The method of Claim 15, wherein the switched-capacitor array comprises a bridge capacitor array, including:

at least first and second array sections;

the first array section associated with the first common node and the second array section associated with [[the]] a second common node;

the second common node separated from the first common node by a series capacitor;

the non-selected array capacitors inclusive of the array capacitors in the second section; and

wherein the compensation capacitor has a value equal to the equivalent capacitance loaded on the first common node from the non-selected array capacitors in the second section.

17. (Original): The method of Claim 16, wherein the compensation capacitor has a parasitic capacitance proportionally equal to the parasitic capacitance of each of the array capacitors based on the relative values thereof.

18. (Previously Presented): The method of Claim 16, wherein at least one of the array capacitors in the first section comprises one of the non-selected array capacitors.

19. (Previously Presented): The method of Claim 18, wherein the at least one of the array capacitors in the first section that comprises one of the non-selected array capacitors comprises the smallest capacitance value in the first section.

20. (Original): The method of Claim 14, wherein the first reference voltage comprises system ground.

21. (Original): The method of Claim 14, wherein the compare reference voltage comprises a common mode reference voltage.

22. (Original): The method of Claim 21, further including the step of generating the common mode voltage with a low impedance common mode driver.

23. (Previously Presented): The method of Claim 22, wherein the step of generating is operable to drive the first common node with the common mode voltage during the sampling phase.

24. (Original): The method of Claim 14, wherein the step of switching with the successive approximation controller is operable to switch all of the switched plates of the array capacitors and the switched plate of the compensation capacitor to the first reference voltage substantially immediately after the sampling phase during a hold phase, and then selectively switching the switched plates of the array capacitors to the second reference voltage in accordance with the successive approximation algorithm and then testing the output of the comparator.

25. (Original): The method of Claim 24, wherein the first reference voltage comprises system ground.